

INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

OCT 23 2003

Docket Number (Optional)
13688

Application Number
09/870,766

Applicant(s)
Richard S. NORMAN et al.

Filing Date
June 1, 2001

Group Art Unit
2661 2664

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
m	1.	U.S. 5,790,539	08-04-1998	Chao et al.	—	—	
	2.	U.S. 5,831,980	11-03-1998	Varma et al.	—	—	
v	3.	U.S. 6,069,895	05-30-2000	Ayandeh	—	—	

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	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
m	4.	EP 0 241 152 A2	10-14-1987	EUROPE	—	—		

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m	5.	NOTANI H ET AL: "An 8*8 ATM switch LSI with shared multi-buffer architecture" PROCEEDINGS OF THE SYMPOSIUM ON VLSI CIRCUITS. SEATTLE, JUNE 4-6, 1992, SYMPOSIUM ON VLSI CIRCUITS, NEW YORK, IEEE, US, 4 June 1992 (1992-06-04), pages 74-75, XP010064987
m	6.	International Search Report PCT/CA02/00810, August 1, 2003

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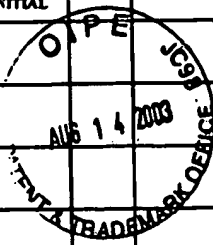
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							YES	NO
<i>m</i>	1.	WO 98/26539	06-18-1998	International	—	—		
<i>m</i>	2.	EP 1 051 001 A2	11-08-2000	Europe	—	—		

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				Filing Date June 1, 2001		Group Art Unit 2661 9664	

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 AUG 28 2001
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	2.	U.S. 5,072,366	10/12/1991	Simcoe			
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							YES	NO

OTHER DOCUMENTS <small>(Including Author, Title, Date, Pertinent Pages, Etc.)</small>		
r	4.	French, R., Architectural Consideration for Internet Routers; retrieved from the internet guideline in file; Internet URL www.cise.ufl.edu/~rfrench , accessed July 23, 2001;
r	5.	Joseph Desposito; Router-On-A-Chip Manages Network Traffic with Wire-Speed QoS; Electronic Design; May 1, 2000; pp 64-65-66;

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Applicant(s) Richard NORMAN et al.		Filing Date June 1, 2001	
Group Art Unit 2664 2664			

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6.		Werner Bux et al.; Technologies and Building Blocks for Fast Packet Forwarding; IEEE Communications Magazine; January 2001; pp. 70-77.
7.		Minagawa, N. et al. ; Dept. of Comput. Scil, University of Electro-Commun. Tokyo, Japan; Implementation of a network switch on chips;(Abstract) Communications, vol. 13, no. 1; retrieved on March 16, 2001 from INSPEC database.
8.		Saturn: a terabit packet switch using dual round-robin; (abstract) Globecom'00 - IEEE, Global Telecommunications Conference; Dept. of Electr. Eng. Polytech, Univ. of Brooklyn, NY, U.S.A.; retrieved on June 4, 2001 from INSPEC database.
9.		Nanette J. Boden et al.; Myrinet - Gigabit-per-Second Local-Area Network [on line]; November 16, 1994 Myricom, Inc.; Internet URL http://www.myrinet.com/research/publications/Hot.ps ; retrieved on March 14, 2001;
10.		Vitesse Semiconductor Corporation [on line] ; Datasheet VSC880; January 5, 2001; pp. 1-20; retrieved on July 23, 2001; Internet URL www.vitesse.com/products/documents.cfm?family=document-id=180 ;
11.		Vitesse Semiconductor Corporation [on line] ; Datasheet VSC870; June 29, 2001; pp. 1-40; retrieved July 23, 2001; Internet URL www.vitesse.com
12.		A New Architecture for Switch and Router Design; PMC-Sierra Inc.; December 22, 1999; Internet URL http://www.pmc-sierra.com/pressRoom/pht/1cs_wp.pdf retrieved on July 4, 2001; pp. 1-8;
13.		Network Processor Designs for Next-Generation Networking Equipment [on line] ; EZ Chip Technologies; Internet URL http://www.ezchip.com/images/pdfs/etchip_white_paper.pdf ; retrieved on July 4, 2001; December 1999; pp.1-4.
14.		Cyrel Minkenberg et al. A combined Input and Output Queued Packet-Switched System Based on Prizma Switch-on-a-Chip Technology; Scalable High-Speed Switches/Routers with QoS Support; IBM Research, Zurich Research Laboratory; IEEE Communications Magazine; December 2000; pp 70-84;
15.		Werner Bux et al.; Technologies and Building Blocks for Fast Packet Forwarding; Telecommunications Networking at the Start of the 21st Century; IEEE Communications Magazine; January 2001; pp 70-77;
16.		Child, J.; Bus-switching chip busts bandwidth barrier [on line] ; Internet URL http://www.computer-design.com/editorial/1995/06/directions/bus.html ; retrieved on March 15, 2001.
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	2.	U.S. Re. 34,755	11/10/1994	Eng et al.	—	—	
	3.	U.S. Re. 34,811	27/12/1994	Eng et al.	—	—	
	4.	U.S. 5,361,257	01/11/1994	Petersen	—	—	
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	8.	U.S. 5,043,980	27/08/1991	Day, Jr. et al.	—	—	
	9.	U.S. 6,144,662	07/11/2000	Colmant et al.	—	—	
	10.	U.S. 5,938,736	17/08/1999	Muller et al.	—	—	
✓	11.	U.S. 5,247,513	21/09/1993	Henrion et al.	—	—	

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m	13.	Nick McKeown et al. "The Tiny Tera: a Packet Switch Core"; Departments of Electrical Engineering and Computer Science, Stanford University; August 1996; http://tiny-tera.stanford.edu/tiny-tera/index.html

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APPLICANT(S)

Richard S. NORMAN et al.

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m	14.	U.S. 6,111,856	29/08/2000	Huterer et al.	—	—	
m	15.	U.s. 5,859,835	12/01/1999	Varma et al.	—	—	

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